

# Claims

- [c1] 1. A chip package structure process, comprising:  
providing a matrix substrate;  
disposing a plurality of chips on the matrix substrate and the chips are electrically connected to the matrix substrate;  
disposing a stiffener on the matrix substrate, wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the matrix substrate;  
providing a molding compound to cover the chips, the matrix substrate, the outer surface and the inner surface of the stiffener; and  
dicing the molding compound, the matrix substrate and the stiffener to form a plurality of chip package structures.
- [c2] 2. The chip package structure process of claim 1, wherein the stiffener has a plurality of openings and locations of the openings correspond to locations of the chips disposed on the matrix substrate.
- [c3] 3. The chip package structure process of claim 1, wherein the inner surface of the stiffener faces the chips.

- [c4] 4. The chip package structure process of claim 1, wherein the stiffener is attached to the matrix substrate through an adhesive.
- [c5] 5. The chip package structure process of claim 1, wherein a plurality of solder balls are formed on the matrix substrate after dicing the molding compound, the matrix substrate and the stiffener.
- [c6] 6. The chip package structure process of claim 1, wherein a plurality of solder balls are formed on the matrix substrate before dicing the molding compound, the matrix substrate and the stiffener.
- [c7] 7. The chip package structure process of claim 1, wherein the chips are attached to the matrix substrate through an adhesive in the step of disposing the plurality of chips and a plurality of wires are formed by wire-bonding to electrically connect the chips and the matrix substrate.
- [c8] 8. The chip package structure process of claim 1, wherein a material of the stiffener is copper.
- [c9] 9. A chip package structure, comprising:
  - a substrate;
  - a chip, disposed on the substrate and electrically con-

nected to the substrate;

a stiffener, disposed on the substrate, wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the substrate; and

a molding compound, covering the chips, the matrix substrate, the outer surface and the inner surface of the stiffener.

[c10] 10. The chip package structure of claim 9, wherein the stiffener has at least an opening and a location of the opening corresponds to a location of the chip disposed on the substrate.

[c11] 11. The chip package structure of claim 9, wherein the inner surface of the stiffener faces the chip.

[c12] 12. The chip package structure of claim 9, wherein the chip package structure further includes a plurality of wires and the chip disposed on the substrate is electrically connected to the substrate through the wires.

[c13] 13. The chip package structure of claim 9, wherein a material of the stiffener is copper.

[c14] 14. A chip package structure, comprising:  
a thin substrate, wherein the thin substrate has a thickness of between about 0.1mm and about 0.5 mm;

a chip, disposed on the thin substrate and electrically connected to the thin substrate;  
a stiffener, disposed on the thin substrate; and  
a molding compound, covering the chips, the thin substrate and the stiffener.

[c15] 15. The chip package structure of claim 14, wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the thin substrate and the molding compound covers the inner surface and the outer surface of the stiffener.

[c16] 16. The chip package structure of claim 14, wherein the inner surface of the stiffener faces the chip.

[c17] 17. The chip package structure of claim 14, wherein the stiffener has at least an opening and a location of the opening corresponds to a location of the chip disposed on the substrate.

[c18] 18. The chip package structure of claim 14, wherein the chip package structure further includes a plurality of wires and the chip disposed on the substrate is electrically connected to the substrate through the wires.

[c19] 19. The chip package structure of claim 14, wherein a material of the stiffener is copper.

- [c20] 20. An stiffener comprises a top portion, a sidewall and a flange portion, wherein the top portion is supported and surrounded by the surrounding sidewall and one side of the sidewall is connected to a periphery of the top portion, while the flange portion is connected to the other side of the sidewall and the flange portion surrounds the sidewall, wherein the sidewall is tilted to the top portion and the flange portion is parallel to the top portion, wherein the stiffener has at least an opening disposed on the top portion of the stiffener.
- [c21] 21. The stiffener of claim 20, wherein the stiffener includes a plurality of openings arranged in arrays on the top portion of the stiffener.
- [c22] 22. The stiffener of claim 20, wherein the flange portion extends outwardly from the sidewall.
- [c23] 23. The stiffener of claim 20, wherein a material of the stiffener is copper.